REMARKS

Claims 1 through 4 are currently pending in the application.

Claim 4 is withdrawn from consideration as being directed to a non-elected invention.

This amendment is in response to the Office Action of November 10, 2005.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Palagonia (U.S. Patent 5,604,377) in view of Nishino (U.S. Patent 5,343,075) and Burns (U.S. Patent 6,049,123)

Claims 1 through 3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Palagonia (U.S. Patent 5,604,377) in view of Nishino (U.S. Patent 5,343,075) and Burns (U.S. Patent 6,049,123). Applicants respectfully traverse this rejection, as hereinafter set forth.

Applicants assert that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicants' disclosure.

Turing to the cited prior art, the Palagonia reference teaches or suggests a packaging scheme for a stack of semiconductor chips. The stack of semiconductor chips is connected to a wiring interface. Separating each of the chips from any adjacent chip is a supporting, insulating interposer. The interposers are cantilevered shelves of a rack. Lead frame fingers contacting solder balls on the semiconductor chips connect the chips to a printed circuit board.

The Nishino reference teaches or suggests a composite stacked semiconductor device having semiconductor devices having external leads projecting from opposite sides thereof in contact with contact plates.

The Burns reference teaches or suggests a stacked semiconductor package including a casing which may be eliminated surrounding a semiconductor die element.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants assert that any combination of the Palagonia reference, the Nishino reference and the Burns reference fails to teach or suggest the claim limitations of the claimed inventions of presently amended independent claims 1 and 3 calling for "providing a plurality of primary integrated circuit packages, each primary integrated circuit package having a plurality of peripheral sides, a top, and a bottom and having a plurality of leads extending from one peripheral side", "providing a cage including an open top, an open bottom, at least three attached adjacent peripheral sides and portions of a fourth peripheral side attached to each of two of the at least three attached adjacent peripheral sides, one side of the attached adjacent peripheral sides having a plurality of conductive buses thereon, the cage enclosing at least three adjacent peripheral sides of the plurality of sides of each primary integrated circuit package of the stacked plurality of primary integrated circuit packages", and "attaching the cage to the substrate, the cage connecting at least one lead extending from a peripheral side of at least one integrated circuit package of the plurality of outer leads of the stacked plurality of primary integrated circuit packages to at least one conductive bus of a plurality of spaced transverse conductive buses". Applicants assert that any combination of the Palagonia reference, the Nishino reference, and Burns reference teaches or suggests the use of a closed cage not having a conductor on the side thereof but an independent conductor contacting the leads of the printed circuit board to which the leads are fixed. Such is not the claimed inventions of presently amended independent claims 1 and 3. Accordingly, any combination of the Palagonia reference, the Nishino reference, and the Burns reference fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 1 and 3. Accordingly, presently amended independent claims 1 and 3 are allowable as well as dependent claim 2.

Additionally, Applicants assert that the sole suggestion for any combination of the Palagonia reference, the Nishino reference, and the Burns reference is solely Applicants' disclosure, not the cited prior art, as the cited prior art contains no suggestion whatsoever for any

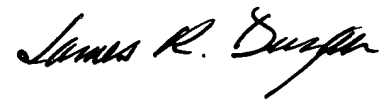
combination thereof. Such is evidenced by the fact that any modification of the Palagonia reference based upon the Nishino reference and the Burns reference clearly destroys the invention of the Palagonia reference because the leads and printed circuit board of the Palagonia reference must be eliminated when the packaged semiconductor die of either Nishino reference or the Burns reference is substituted for the unpackaged semiconductor chip of Palagonia. Therefore, any combination of the Palagonia reference, the Nishino reference, and the Burns reference fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed inventions of presently amended independent claims 1 and 3. Accordingly, presently amended independent claims 1 and 3 are allowable as well as dependent claim 2.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicants have amended the claimed invention to clearly distinguish over the cited prior art.

Applicants submit that claims 1 through 3 are clearly allowable over the cited prior art.

Applicants request the allowance of claims 1 through 3 and the case passed for issue.

Respectfully submitted,



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